QUARTERLY PROGRESS REPORT

(2)

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DEFENSE ADVACED RESEARCH PROJECTS AGENCY
DEFENSE SCIENCES OFFICE

RF VACUUM MICROELECTRONICS
ARPA ORDER No. 8162

ISSUED BY DARPA/CMO UNDER CONTRACT No. MDA972-91-C-0032

Raytheon Co.
Lexington

I. EXECUTIVE SUMMARY

Raytheon

VHF micro-triode (cylindrical) wafers started

Design for planar triode complete, masks received

Planar triode wafers started

VHF test parts for planar diode designed and ordered

New evaporator parts received and final assembly started

Improved moly tips with "double evaporation"

Achieved 25 μA/tip emission from 100 tip array

Cornell

Improved control and yield on silicon tips

Lowered work function by "metalization of tips"

Designed mask to be compatible with Raytheon test stand

II. MILESTONES STATUS

	Completion Date Original	Act/Est
1. Moly Tip Field Emitter		
1.1 Process enhancement	2/93	
1.2 Leakage current suppression	7/92	10/92
1.3 Series resistor development	9/92	11/92
1.4 Alternative Emitter materials	2/93	
2. Wing Field Emitter		
2.1 Process development	4/92	stopped
2.2 Electrical tests	6/92	stopped
3. DC/Low Frequency Test		
3.1 Improve bakeout and turn on proc.	12/91	12/91
3.2 Life tests	2/93	
4. High Frequency Design/Fab		
4.1 VHF micro-triode (cylindrical) design/fab	5/92	8/92
4.2 Planar micro-triode design/fab	5/92	8/92
5. High Frequency Test		
5.1 Test VHF micro-triode	8/92	9/92
5.2 Test planar micro-triode	8/92	9/92
6. Silicon Tip Development	2/93	
7. Cantilevered Gate	2/93	

III. TECHNICAL PROGRESS

Raytheon

1.1 An improvement has been made in the process that makes better tips with lower turn-on voltage. Our standard process has one moly evaporation step. If the excess metal is removed and the whole process is repeated, we are able to better position the top of the tip and have a smaller curvature of radius at the tip. Turn on voltages have been observed as low as 30 volts.

A set of wafers were run on quartz substrate instead of silicon. The processing was successful and the tips emitted. There appears to be a greater outgassing problem with the quartz that limited the maximum current. This problem is under active investigation. On possible solution is the cap the whole wafer with a layer of LTO.

While looking at the gate moly on the Auger system for other reasons, a high nitrogen content was observed. Methods for removal during the processing of wafers by hydrogen and vacuum anneals will be investigated.

1.2 The leakage problem between the gate and emitter level that seemed to be solved last quarter has intermittently recurred. The residual metal containing organic film, produced during the reactive ion etch of the cavities, left on the side wall is the suspected culprit. Raytheon is working with a third party vendor, EKC to solve this problem.

1.3 Three methods of making series resistors are under study (polysilicon, sputtered TaO_xN_y, and co-evaporated cermat (SiO/Mo)). The initial polysilicon resistors looked like back to back diodes with the knee in the anticipated operating regime. Therefore, the other two types will be fabricated and tested next quarter.

1.4 A set of wafers were run with Hafnium coated (5A) tips. Instead of the expected lower turn on voltage, an increase of 10 volts over that of moly was found.

The carbide targets (Zirconium, Hafnium, and Tantalum) were ordered and received. ZrC was deposited on a planar surface and is currently under analysis.

3.1 A MAC Quadra computer was purchased (internal funds) to control and monitor the FEA test stand. The electronics on the test stand have been upgraded to include IEEE-488.2 computer interfaces. The equipment control software package LabView was purchased from National Instruments. Programs has been developed to monitor the long bakeouts. Further software

enhancements will include active control of the bakeout, automatic IV curve acquisition, lifetest monitoring, etc.

3.2 No long lifetests have been run since the test stand is needed for all the other testing. The best result has been a 100 tip array run for 24 hours at 1 μA/tip with no measurable degradation. This test was terminated to push the device to higher currents.

4.1-2 The masks for both high frequency designs (cylindrical and planar) were received and wafer processing was started. The first lots should be available for test in August 1992.

The layout for the planar chip is shown if Figure 1. There are 11 test structure on the chip. A 2-port RF cathode runs across the top. There are six 1-port RF cathodes, three per side. Four cold test structure are located in the middle. From top to bottom they are a RF probe calibration short and open, a capacitor (no tips or holes) and a complete emitter. The big pads on the sides are bonded to an alumina with 50 ohm lines that transition to a coax line. The small pads on all the structures are for cold test the RF probes.

The two port structure will allow for external RF tuning of the cathode. The topology of this structure is similar to that of the cylindrical triode. The one port structures are two sizes with varying density of tips.

Both design's will first be tested DC. A special alumina that can hold both styles of chips was designed and ordered and should be received the first week of August.

5.1 All the prime parts for the VHF micro-triode have been designed and ordered. Fifty percent have been received with the balance due by the middle of August. Assembly and test will follow.

5.2 The alumina for the planar micro-triode has been designed, ordered and should be received by the end of August. Two vacuum flanges with high frequency bakable 50 ohm (0.141 inch) feedthru's were designed and ordered and should be received by the third week in August. The upper frequency of this holder should be above 2 GHz. The input and output 50 ohm lines will be characterized in both phase and amplitude (S-parameters). This will allow for de-embedding of the measured RF performance of the assembly back down to the chip. From this data, a true value of F_t can be obtained. All the other RF test

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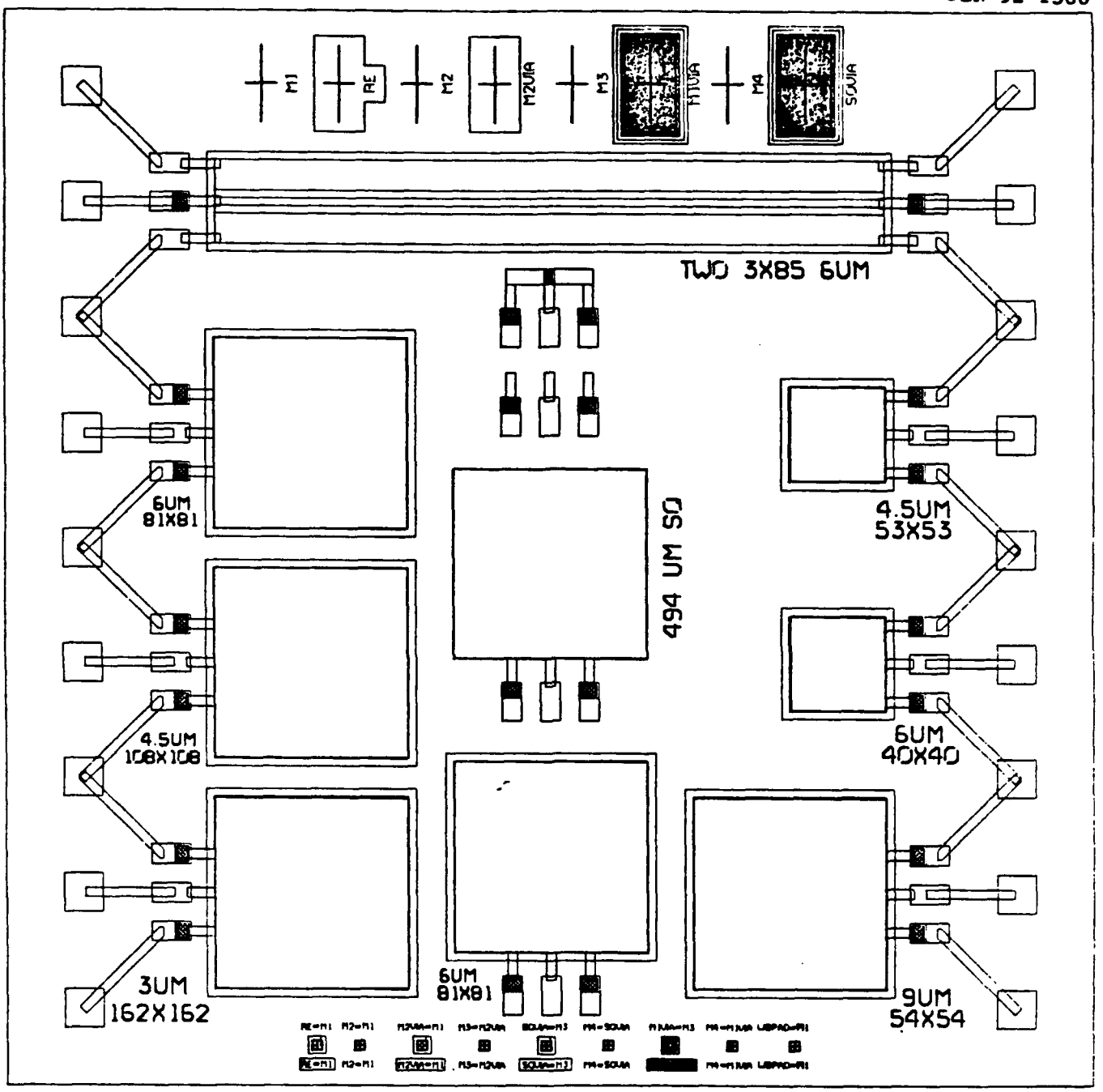


Figure 1. Layout for the Planar Chip.

equipment (vector network analyzer's, filters, tuners, bias T's, etc.,) has be purchased or is available for the initial testing. This work should commence in September.

Cornell

6 Cornell has developed a procedure for "metalization" of the silicon tips (internal funding). Initial tests indicate these tips have a turn on voltage substantially lower than that of bare Si tips. More quantitative results will be available next quarter after this process has been used on DARPA funded wafers.

The control of the cathode aperture and tip height has been improved in the oxidation process for making Si tips. Figure 2 shows SEMs of some typical results.

Currents obtained from these tips have not been has high as the moly. However, there is no bakeout capability at Cornell. These cathodes will be tested at Raytheon next quarter.

The Cornell masks were modified to be compatible with Raytheon's planar triode design. This will allow for RF probing, DC testing, and RF frequency testing of the Cornell chips at Raytheon.

OTHER

The new evaporator (purchased with internal funds) should be ready to use in the August time frame. This represents a one month slip from our original schedule. The delay was due to problems our vendors encountered in fabrication of the main chamber. This new evaporator should reduce our processing time from six weeks to four weeks and give us increased versatility and better control of this critical process step.

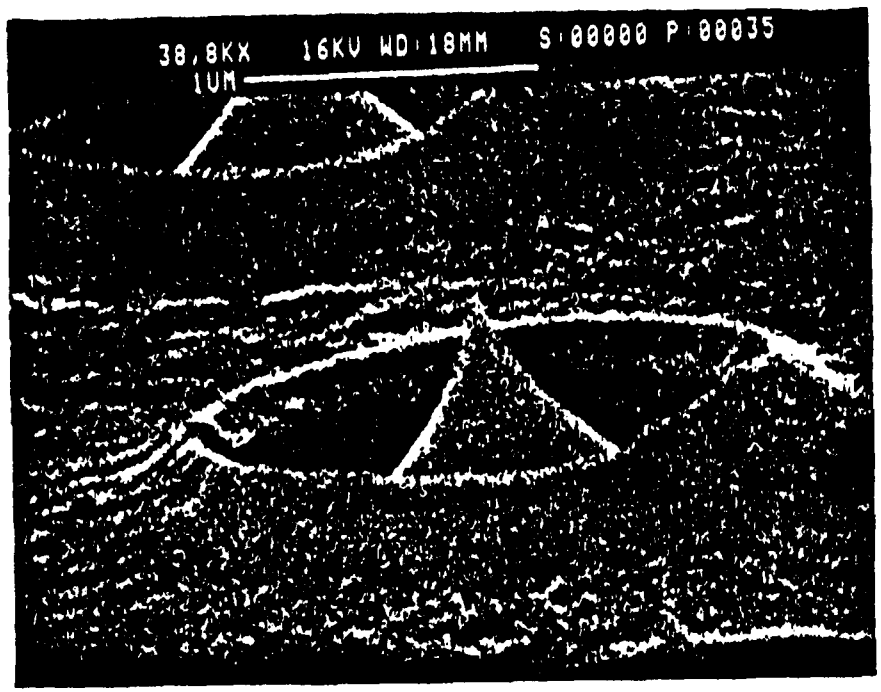
Some un-gated tips were obtained from SAIC.

Two cathodes were obtained from SRI. One was processed by SRI and the other has not been turned on. We want to see if we can observe "field forming". This reported effect has not been observed at Raytheon.

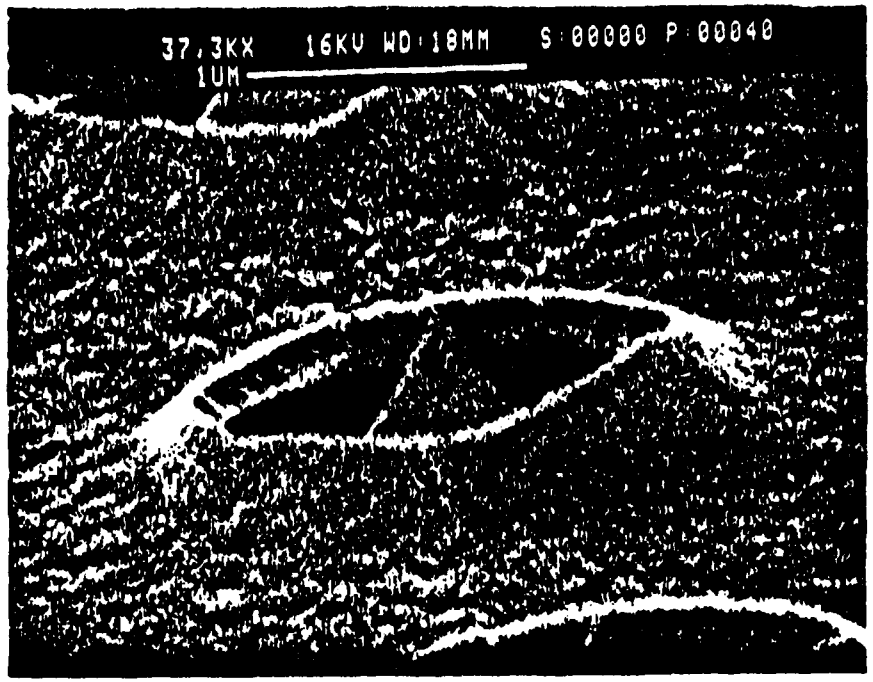
Micron Corporation plans to test some of their silicon chips on the Raytheon test stand next quarter.

Dr. Wolfgang Feist retired at the end of June.

IV. FISCAL STATUS



Cathode Apex ≈ 4000 Å Above the Aperture



Cathode Apex ≈ 2500 Å Above the Aperture

Figure 2. Tip Height Dependence on Cap Diameter.

IV FISCAL STATUS

CONTRACT NO: MDA972-91-C-0032
CONTR. TITLE: RF VACUUM MICROELECTRONICS
CONTRACTOR: RAYTHEON CO., RESEARCH DIV.

DATE PREPARED: 24-Jul-92
REPORT PERIOD: 05/25/92-06/28/92

FUNDS AND MANHOUR EXPENDITURE REPORT

CONTRACT VALUE:	$1,095,328
CURRENT FUNDING (cell):	$762,000
NEG. FEE RATE:	0.0%

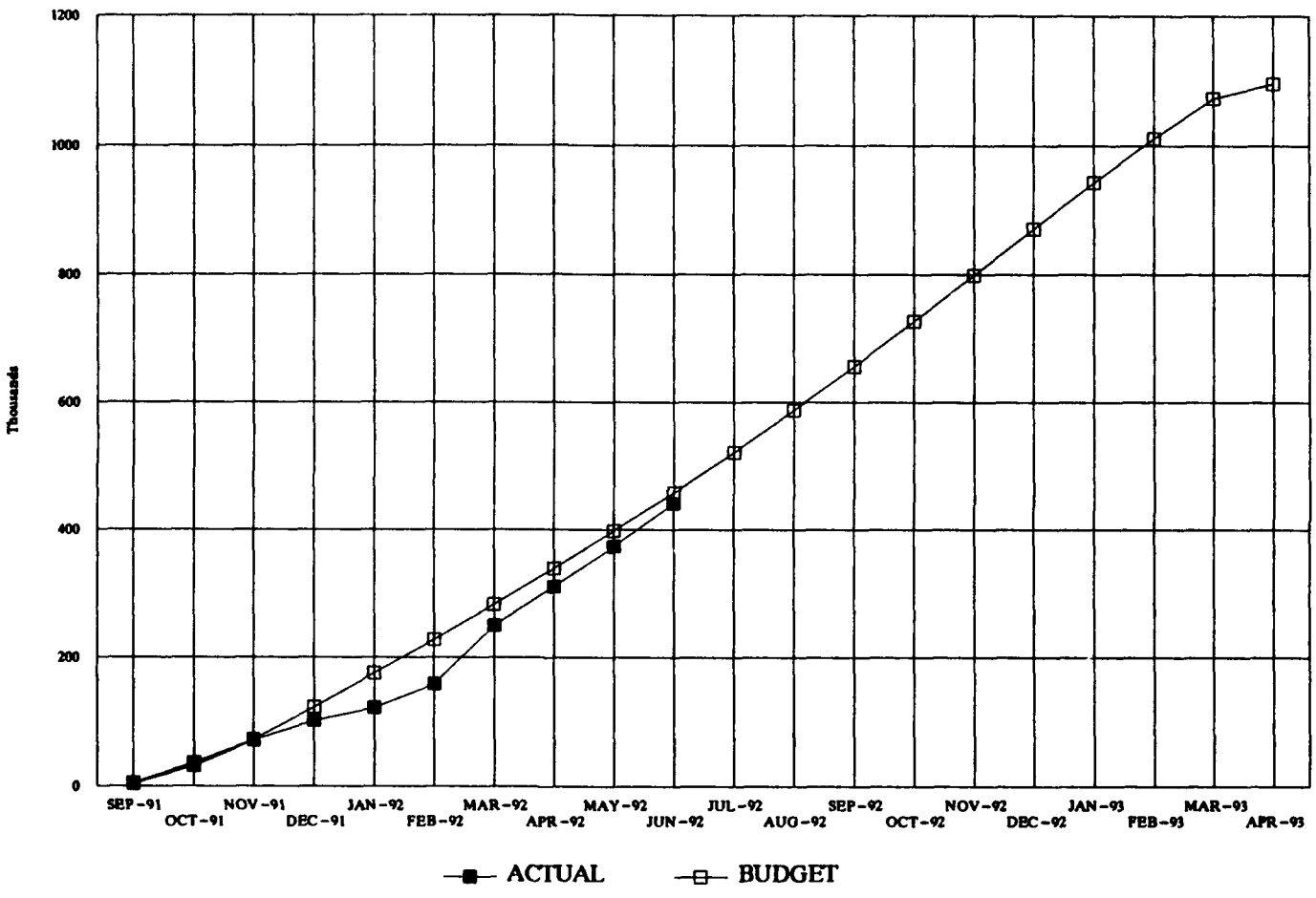
	CONTRACT VALUE	REPORTING MO. EXPEN-DITURES	CUMULATIVE EXPEND. TO DATE	% $ VALUE	COST TO COMPLETE ESTIMATE	LATEST COST ESTIMATE	PREVIOUS COST ESTIMATE
A	B	C	D	E	F	G	H
TOTAL PRIME LABOR HOURS	7,467	350	3,012		4,455	7,467	
TOTAL PRIME LABOR	$203,891	$8,767	$87,142		$116,749	$203,891	0
LABOR OVERHEAD	$362,926	$15,395	$153,706		$209,220	$362,926	0
TOTAL LABOR & OVERHEAD	$566,817	$24,162	$240,848		$325,969	$566,817	0
MATERIALS	$220,841	$26,084	$100,445		$120,396	$220,841	0
ODC	$830	$179	$1,342		($512)	$830	0
IWR	$135,944	$6,146	$27,680		$108,264	$135,944	0
PRODUCT COST	$924,432	$56,571	$370,315		$554,117	$924,432	0
G & A	$148,407	$9,068	$59,945		$88,462	$148,407	0
COM	$22,489	$1,002	$10,324		$12,165	$22,489	0
TOTAL COST LEVEL	$1,095,328	$66,641	$440,584		$654,744	$1,095,328	0
FEE	$0	$0	$0		$0	$0	0
TOTAL CONTRACT PRICE	$1,095,328	$66,641	$440,584	40.22%	$654,744	$1,095,328	0
OUTSTANDING COMMIT.		$106,159	$106,159				
TOTAL COMMIT & EXPEND.	$1,095,328	$172,800	$546,743	49.92%	$654,744	$1,095,328	0

EXPENDITURES THIS QUARTER:	$190,748
TOTAL EXPENDITURES TO DATE:	$440,584
PROJECTED EXPENDITURES:	
07/92 - 09/92:	$215,916
10/92 - 12/92:	$215,100
01/93 - 03/93:	$201,200
04/93 - 06/93:	$22,528
TOTAL FY92 EXPENDITURES:	$656,500
1) IS CURRENT FUNDING SUFFICIENT (Y/N):	YES
2) WHAT IS FY93's FUNDING REQUIREMENT?:	$1,095,328
3) IS ALL DATA CROSS REFERENCED?:	YES

RF Vacuum Microelectronics

DATE	ACTUAL	BUDGET
SEP-91	4,473	4,500
OCT-91	31,728	35,700
NOV-91	71,413	72,400
DEC-91	101,907	122,600
JAN-92	121,800	175,100
FEB-92	158,722	228,100
MAR-92	249,836	283,100
APR-92	311,137	339,400
MAY-92	373,943	397,700
JUN-92	440,584	458,100
JUL-92		521,600
AUG-92		587,700
SEP-92		656,500
OCT-92		727,200
NOV-92		799,300
DEC-92		871,600
JAN-93		943,500
FEB-93		1,011,500
MAR-93		1,072,800
APR-93		1,095,328

Funding @ TCL = $762,000
Basic Value @ TCL = $1,095,328



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V. PROBLEM AREAS

1. Work on the circular edge emitters (wings) was discontinued due to poor performance.

2. The gate to emitter leakage problem requires more work

VI. VISITS AND TECHNICAL PRESENTATIONS

None